REMARKS

New claims 29 and 30 have been added, and therefore claims 13 to 30 are presently pending.

Applicant respectfully requests reconsideration of the present application in view of this response.

With respect to page two (2) of the Office Action, claims 13 to 28 were rejected under the second paragraph of 35 U.S.C. §112 as indefinite. First, the Office Action asserts that the recited text of "high" in "high temperature" in claims 13, 17 and 18 is a relative term which renders the claim indefinite, and that "the specification does not provide a standard for ascertaining the requisite degree."

It is respectfully submitted that the recited text of "high temperature" in claims 13, 17 and 18 would be understood by those of ordinary skill in the art in light of the clear guidance on page 3 of the specification that "[t]he diffusion process, carried out after the coating with doped glass layers, takes place in a diffusion oven *at a temperature of 1200 to 1280 degrees* Celsius." (See Specification page 3, lines 21 to 22) (emphasis added). It is respectfully submitted that this unambiguous statement in the specification would inform those of skill in the art what is meant by "high temperature" in claims 13, 17 and 18, and that these claims are therefore definite with respect to this recited text.

It is further stated in the Office Action that the recited text "deep" in claim 13 is a relative term which renders the claim indefinite. As this term has been removed from the claim, it is respectfully submitted that claim 13 is definite and that the definiteness rejection should therefore be withdrawn.

As regards claims 19, 20, 23 and 24, the Office Action asserts that these claims are indefinite due to informalities concerning use of the article "a" versus "the". As the informalities have been removed in accordance with the suggestions set forth in the Office Action, it is respectfully submitted that claims 19, 20, 23 and 24 are definite, and that the definiteness rejection should therefore be withdrawn with respect to these claims as well.

On page three (3) of the Office Action, claims 13, 14, 16 to 19, 21 and 25 were rejected under 35 U.S.C. §102(b) as anticipated by Rosnowski, U.S. Patent No. 4,099,997.

It is axiomatic that for a claim to be anticipated under 35 U.S.C. § 102(b), a single prior art reference must disclose each and every element of the claim in *exactly the same way*. (See Lindeman Machinenfabrik v. Am. Hoist and Derrick, 730 F.2d 1452, 1458 (Fed. Cir.

1984) (emphasis added)). It is respectfully submitted that Rosnowski does not meet this legal standard because it does not disclose each and every feature of claim 13 in exactly the same way.

Claim 13 recites the features of applying a solid glass layer provided with a dopant on at least one of two sides of the semiconductor wafer and heating the semiconductor wafer to a high temperature so that the dopant from the solid glass layer penetrates into the semiconductor wafer to produce at least one doped region.

The Rosnowski reference purportedly relates to a method for fabricating thyristor devices in which borosilicate layers are deposited upon a wafer. (See Rosnowski, col. 2, lines 18-26). After masking the borosilcate layers with silicon dioxide, aluminum impurities are purportedly diffused into the wafer "by the use of any known method." (See Rosnowski, col. 2, line 65 to col. 3, line 2). As further stated, "during the diffusion process some of the boron from the layers 18 and 19," the borosilicate layers have been "driven into the wafer 12 and therefore there also exists, at this point, a surface concentration . . . which penetrates into the wafer 12 beneath the unexposed portions 26 to a depth of about 3 micrometers" -- which is less than 2 percent of the thickness of the wafer. (See Rosnowski col. 3, lines 12-18; col. 2, line 8.)

With regard to this surface diffusion, there is no mention of or reference to the temperature at which this process occurs, or its duration. Only after the borosilicate glass layers are *removed* is the wafer then "heated to a temperature at which the first [boron] and second [aluminum] impurities are driven *further thereinto*." (See Rosnowski, col. 3, lines 40-44) (emphasis added). The temperature of this post-removal heating is purported to be in the range of 1200 to 1300 degrees centigrade, and the duration of this heating is purported to be between 140 and 20 hours. (See Rosnowski, col. 3, lines 50-52). Since this later high temperature[1] heating process takes place after the doped glass layer has been removed, Rosnowski simply does not identically describe (or even suggest) heating the semiconductor wafer to a high temperature so that the dopant **from the solid glass layer** penetrates into the semiconductor wafer. That is, dopants do not diffuse from the solid glass layer to penetrate the semiconductor wafer to produce a doped region when heated to a high temperature, as recited in claim 13. For at least this reason, it is respectfully submitted that Rosnowski does not anticipate claim 13.

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[1] The meaning of "high" temperature being understood by those of ordinary skilled in the art in light of the specification as explained above.

As claims 14, 16 to 19, 21 and 25 depend, directly or indirectly, from claim 13, they are not anticipated by Rosnowski for at least the same reasons discussed with respect to claim 13.

On page four (4) of the Office Action, claims 15, 22 and 28 were rejected under 35 U.S.C. §103(a) as unpatentable over Rosnowski in view of Schwalke, U.S. Patent No. 5,496,765.

To reject a claim as obvious under 35 U.S.C. § 103, the prior art must disclose or suggest each claim element and it must also suggest combining the elements in the manner contemplated by the claim. (See Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), cert. denied, 111 S. Ct. 296 (1990)).

Each of claims 15, 22 and 28 depend from and incorporate the features of independent claim 13. The secondary Schwalke reference purportedly relates to a method for producing an insulating trench in an SOI substrate, and refers to diffusion of dopants laterally through side walls of an etch. As characterized in the reference, the dopant diffuses from a glass layer through intermediary silicon dioxide films to a monocrystalline layer and does not diffuse to the substrate layer. (See Schwalke, col. 4, lines 38 to 47). Since Schwalke also does not disclose or suggest heating the semiconductor wafer to a high temperature so that the dopant from the solid glass layer penetrates *into the semiconductor wafer* (i.e., the substrate) as recited in claim 13, it does not cure the critical deficiencies of the primary Rosnowski reference discussed above, and therefore the references relied upon do not disclose or suggest each of the features of claims 15, 22 and 28 as required. For at least this reason, it is respectfully submitted that the obviousness rejection of claims 15, 22 and 28 should be withdrawn.

On page five (5) of the Office Action, claims 20, 23 and 24 were rejected under 35 U.S.C. §103(a) as unpatentable over Rosnowski in view of Barden et al., U.S. Patent No. 4,889,492.

The Barden reference purportedly concerns a method for fabricating trench capacitors. (See Barden, Abstract). Like the Rosnowski reference and unlike the recited method of claim 13, Barden refers to a two-step process of producing a primer doped region with a doped glass layer in place and then producing an extended doped region by diffusion *after the doped glass layer has been removed.* (See Barden, col. 4, lines 58 to 60). Moreover, Barden does not disclose or suggest heating the semiconductor wafer to a high temperature while the doped glass layer is in place. For at least these reasons, Barden does not cure the critical

deficiencies of the primary reference, and claims 20, 23 and 24 are therefore allowable over the references relied upon.

As further regards claim 20, it recites the feature that the solid glass layer is applied both on the front side of the semiconductor wafer and on the back side of the semiconductor wafer, and that a doping type of the dopant on the back side is opposite compared to the doping type of the dopant on the front side. The Office Action admits that the primary Rosnowski reference does not disclose or suggest this feature. However, Barden also does not disclose or suggest applying a glass layer on both the front and back sides of the semiconductor wafer. The layers (54/60) referred to in the Office Action are both applied on the top (front) side of the substrate as clearly indicated in Figures 4 and 6, which indicate layers 54 and 60 in the same respective positions with respect to the semiconductor wafer. For this additional reason, claim 20 is allowable over the references relied upon.

In light of the foregoing, it is respectfully submitted the obviousness rejection of claims 20, 23 and 24 should be withdrawn.

On page six (6) of the Office Action, claims 26 and 27 were rejected under 35 U.S.C. §103(a) as unpatentable over Rosnowski in view of Shinohara, JP 59-80928.

The Shinohara reference purportedly refers to forming a non-doped glass layer over a doped substrate. It is respectfully submitted, however, that any review of the Shinohara reference makes plain that it simply does not disclose or suggest heating the semiconductor wafer to a high temperature so that the dopant from the solid glass layer penetrates into the semiconductor wafer as recited in claim 13. Accordingly, it does not cure the critical deficiencies of the primary Rosnowski reference. It is therefore respectfully submitted that the obviousness rejection of claims 26 and 27 should be withdrawn.

CONCLUSION

In view of all the above, it is believed that rejections of claims 13 to 28 have been obviated, and that currently pending claims 13 to 30 are allowable. It is therefore respectfully requested that the rejections be reconsidered and withdrawn, and that the present application issue as early as possible.

Respectfully submitted,

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AMENDMENT VERSION WITH MARKINGS

IN THE CLAIMS:

Please add new claims 29 and 30 as indicated above, and please amend without prejudice the claims as follows:

13. (Amended) A method for producing a semiconductor component in which at least one doped region is introduced into a semiconductor wafer, comprising the steps of:

applying a solid glass layer provided with a dopant on at least one of two sides of the semiconductor wafer;

heating the semiconductor wafer to a high temperature so that the dopant from the solid glass layer penetrates [deep] into the semiconductor wafer to produce the at least one doped region;

removing the solid glass layer; and

providing [a] the dopant at a dosage of at least $10^{17}/cm^2$ in the at least one doped region.

19. (Amended) The method according to claim 13, wherein:

the solid glass layer is applied both on [a] the front side of the semiconductor wafer and on [a] the back side of the semiconductor wafer, a doping type of the dopant on the back side being the same compared to [a] the doping type of the dopant on the front side.

20. (Amended) The method according to claim 13, wherein:

the solid glass layer is applied both on [a] the front side of the semiconductor wafer and on [a] the back side of the semiconductor wafer, a doping type of the dopant on the back side being opposite compared to [a] the doping type of the dopant on the front side.

23. (Amended) The method according to claim 21, wherein:

the dopant constituent of the solid glass layer on [a] the front side of the semiconductor wafer is different from the dopant constituent of the solid glass layer on [a] the back side of the semiconductor wafer.

24. (Amended) The method according to claim 22, wherein:

the dopant constituent of the solid glass layer on [a] the front side of the semiconductor wafer is different from the dopant constituent of the solid glass layer on [a] the back side of the semiconductor wafer.